103-2 大葉大學 完整版課綱 - 上課進度

上課進度		分配時數(%)				
週次	教學內容	講授	示範	習作	實驗	其他
1	Introduction to chip design & 智財權宣導(含告知學生應使用正版教科書)	0	0	0	0	0
2	FPGA/CPLD General Architectures	0	0	0	0	0
3	Introduction to VHDL Design Methodology	0	0	0	0	0
4	Basics of Combinatorial Logic Design-1	0	0	0	0	0
5	Basics of Combinatorial Logic Design-2	0	0	0	0	0
6	Gate Level Functional Simulation	0	0	0	0	0
7	Chip Level Functional Verification	0	0	0	0	0
8	Basics of Sequential Logic Design I:	0	0	0	0	0
9	期中考試	0	0	0	0	0
10	Registers, Counters, Timers-1	0	0	0	0	0
11	Registers, Counters, Timers-2	0	0	0	0	0
12	Basics of Sequential Logic Design II:	0	0	0	0	0
13	Process, System design, State Machine Logic	0	0	0	0	0
14	Project Demonstration I :	0	0	0	0	0
15	Printer port interface, Electronic clock, Security lock	0	0	0	0	0
16	Project Demonstration II:	0	0	0	0	0
17	Motion control project	0	0	0	0	0
18	期末專題報告與實作展示	0	0	0	0	0