97-2 大葉大學 完整版課綱 - 上課進度

上課進度		分配時數(%)				
週次	教學內容	講授	示範	習作	實驗	其他
1	Introduction to Digital Systems and VLSI	100	0	0	0	0
2	Introduction to CAD Systems and Algorithms	100	0	0	0	0
3	Introduction to CAD Systems and Algorithms	100	0	0	0	0
4	Introduction to VLSI Design Methodologies	100	0	0	0	0
5	Transistor Level Design	50	20	30	0	0
6	Transistor Level Design	50	20	30	0	0
7	Gate Level Design	50	20	30	0	0
8	Gate Level Design	50	20	30	0	0
9	Midterm	0	0	0	0	100
10	Combinational Logic Networks	50	20	30	0	0
11	Sequential Logic Networks	50	20	30	0	0
12	Subsystem Design	50	20	30	0	0
13	Subsystem Design	50	20	30	0	0
14	Architecture Level Design	50	20	30	0	0
15	Architecture Level Design	50	20	30	0	0
16	Chip Level Design	50	20	30	0	0
17	Chip Level Design	50	20	30	0	0