97-2 大葉大學 完整版課綱 - 上課進度

上課進度		分配時數(%)				
週次	教學內容	講授	示範	習作	實驗	其他
1	Pure Behavioral stage of the two-state division machine	66		34		
2	Mixed stage of the two-state division machine	66		34		
3	Pure structural stage of the two state division machine	66		34		
4	Hierarchical refinement of the controller	66		34		
5	Structure of the machine	66		34		
6	Behavioral fetch/execute	66		34		
7	Mixed fetch/execute	66		34		
8	Memory hierarchy	66		34		
9	PDP-8 architecture	66		34		
10	Implement an PDP-8 processor by using Verilog HDL	66		34		
11	Implement an PDP-8 processor by using Verilog HDL	66		34		
12	Implement an PDP-8 processor by using Verilog HDL	66		34		