99-1 Preliminary Syllabus, Da-Yeh Univ

Information			
Title	超大型積體電路設計	Serial No. / ID	1779 / EEI3040
Dept.	電機工程學系	School System / Class	大學日間部3年1班
Lecturer	張永平	Full or Part-time	兼任
Required / Credit	Optinal / 3	Graduate Class	No
Time / Place	(四)9AB / H726	Language	Chinese

Introduction

Good understanding the design techniques of modern VLSI design including transistor modeling, circuit-level scheme, architecture-level scheme, full-custom as well as cell-based design flow through the representative case studies of the multimedia-communications systems.

Outline

TBA

Prerequisite

Electronics
Design of Electronic Circuits