

99-1 Preliminary Syllabus, Da-Yeh Univ

Information			
Title	系統晶片設計	Serial No. / ID	1165 / EGR5358
Dept.	電機工程學系碩士班	School System / Class	研究所碩士班1年1班
Lecturer	陳慶順	Full or Part-time	專任
Required / Credit	Optinal / 3	Graduate Class	No
Time / Place	(二)789 / H726	Language	Chinese

Introduction
This course is intended to study System-on-Chip computing for ASICs and FPGAs including processor design and sw/hw co-design in association with Verilog HDL.

Outline
1.Introduction to SOC 2.SOC Design Flow & Tools 3.RISC Processor Design 4.Hardware/Software Co-design 5.Multi-processor Design 6.Case Study: Childish Multiplier

Prerequisite
Computer Architecture Verilog Hardware Description Language Digital Logic