98-2 Preliminary Syllabus, Da-Yeh Univ

Information			
Title	計算機設計	Serial No. / ID	0613 / EEI4177
Dept.	電機工程學系	School System / Class	大學日間部4年1班
Lecturer	陳慶順	Full or Part-time	專任
Required / Credit	Optinal / 3	Graduate Class	Yes
Time / Place	(一)89A / H731	Language	Chinese

Introduction

This course is intended to study computer architectures that utilize ASM design and to implement a childish multiplier processor by using Verilog HDL.

Outline

Intrduction of ASM and Verilog HDL.
Three Stages for Verilog Design of a Division Machine.

Prerequisite

Computer Architecture
Verilog Hardware Description Language
Digital Logic