

98-1 Preliminary Syllabus, Da-Yeh Univ

Information			
Title	硬體描述語言	Serial No. / ID	1267 / IF13094
Dept.	資訊工程學系	School System / Class	大學日間部3年3班
Lecturer	林浩仁	Full or Part-time	兼任
Required / Credit	Optinal / 3	Graduate Class	NO
Time / Place	(一)89AB / H708	Language	Chinese

Introduction	
NA	

Outline	
unit 1 Overview of Sequential Circuit Design unit 2 Overview of Digital Design with Verilog HDL unit 3 Verilog Overview unit 4 Some Examples unit 5 Modules and Ports unit 6 Gate-Level Modeling unit 7 Dataflow Modeling unit 8 Behavioral Modeling unit 9 Tasks and Functions unit 10 Timing and Delays unit 11 Useful Modeling Techniques unit 12 Switch-Level Modeling unit 13 User-Defined Primitives	

Prerequisite	
NA	