97-2 Preliminary Syllabus, Da-Yeh Univ

Information			
Title	雛形晶片設計	Serial No. / ID	2453 / IFI3098
Dept.	資訊工程學系	School System / Class	大學日間部4年1班
Lecturer	林浩仁	Full or Part-time	兼任
Required / Credit	Optinal / 3	Graduate Class	Yes
Time / Place	(五)5678 / H708	Language	Chinese

Introduction

NA

Outline

Unit 1 FPGA Architecutre and Design Flow
Unit 2 FPGA Implementation
Unit 3 RTL Coding for FPGA
Unit 4 FPGA design for synthesis
Unit 5 FPGA implementation platform
Unit 6 Case Study

Prerequisite

NA