97-2 Preliminary Syllabus, Da-Yeh Univ

Information

Title	FPGA	Serial No. / ID	1935 / EDR 5074
Dept.		School System / Class	1 1
Lecturer		Full or Part-time	
Required / Credit	Optinal / 3	Graduate Class	NO
Time / Place	( )567 / H371	Language	Chinese

Introduction

This course emphasizes on both theory and practice of FPGA IC design in equality, and it also provides any needed concepts of VHDL on FPGA chip design. Additionally, EDA software like Xilinx ISE and related FPGA modules will be introduced to students. Hence, after finishing the lessons, I believe the students to take this course will be capable of being skillful in IC design.

Outline

Introduction to VHDL Design Methodology
Basics of Combinatorial Logic Design
Gate Level Functional Simulation
Chip Level Functional Verification
Basics of Sequential Logic Design I:
Registers, Counters, Timers
Basics of Sequential Logic Design II:
Process, System design, State Machine Logic
Project Demonstration: Electronic clock, Security lock

Prerequisite

Digital logic design
Electronics