97-1 Preliminary Syllabus, Da-Yeh Univ

Information			
Title	FPGA系統設計	Serial No. / ID	2449 / IFR5121
Dept.	資訊工程學系碩士班	School System / Class	研究所碩士班1年1班
Lecturer	林浩仁	Full or Part-time	兼任
Required / Credit	Optinal / 3	Graduate Class	NO
Time / Place	(一)34 / H705 (四)67 / H705	Language	Chinese

Introduction

NA

Outline

Unit 1 RTL Coding for FPGA
Unit 2 FPGA Architecutre and Design Flow
Unit 3 FPGA Implementation
Unit 4 FPGA design for synthesis
Unit 5 FPGA implementation platform
Unit 6 Case Study

Prerequisite

NA