

97-1 Preliminary Syllabus, Da-Yeh Univ

| Information | | | |
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| Title | 計算機結構與設計 | Serial No. / ID | 1136 / EGR5142 |
| Dept. | 電機工程學系碩士班 | School System / Class | 研究所碩士班1年1班 |
| Lecturer | 陳慶順 | Full or Part-time | 專任 |
| Required / Credit | Optinal / 3 | Graduate Class | NO |
| Time / Place | (二)9AB / H726 | Language | Chinese |

| Introduction |
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| This course is intended to study computer architectures that utilize ASM design and to implement a childish multiplier processor by using Verilog HDL. |

| Outline |
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| Intrduction of ASM and Verilog HDL. Three Stages for Verilog Design of a Division Machine. |

| Prerequisite |
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| Computer Architecture Verilog Hardware De s c r i p t i o n Language Digital Logic |