97-1 Preliminary Syllabus, Da-Yeh Univ

Information			
Title	超大型積體電路技術	Serial No. / ID	0673 / EEI4012
Dept.	電機工程學系	School System / Class	大學日間部4年1班
Lecturer	李世鴻	Full or Part-time	專任
Required / Credit	Optinal / 3	Graduate Class	Yes
Time / Place	(三)12 / P301 (五)1 / H202	Language	Chinese

Introduction

To furnish the students with the understanding of the principles, technologies, and equipments involved in the fabrication of very-large-scale intergrated circuits.

Outline

1. Vacuum and Plasma; 2. Wafer; 3. Thin Film Deposition; 4. Physical Vapor Deposition; 5. Chemical Vapor Deposition; 6. Photolithography; 7. Thermal Oxdation; 8. Etching; 9. Thermal Diffusion; 10. Ion Implantation.

Prerequisite

Solid State Electronics