97-1 Preliminary Syllabus, Da-Yeh Univ

Information			
Title	Verilog硬體描述語言	Serial No. / ID	0658 / EEI3106
Dept.	電機工程學系	School System / Class	大學日間部3年1班
Lecturer	陳慶順	Full or Part-time	專任
Required / Credit	Optinal / 3	Graduate Class	NO
Time / Place	(一)9AB / H731	Language	Chinese

Introduction

This course is intended to introduce and show students how to write hardware de s c r i p t ion in Verilog, and how to write them in a synthesis-friendly style.

Outline

1. A Tutorial Introduction
2. Logic Synthesis
3. Behavioral Modeling
4. Concurrent Processes
5. Module Hierarchy
6. Logic Level Modeling
7. Cycle-Accurate Specification
8. Advanced Timing

Prerequisite

Computer Programming Language
Digital Logic