102-2 Preliminary Syllabus, Da-Yeh Univ

Information			
Title	硬體描述語言	Serial No. / ID	0882 / EEI2038
Dept.	電機工程學系	School System / Class	大學日間部2年1班
Lecturer	陳慶順	Full or Part-time	專任
Required / Credit	Optinal / 3	Graduate Class	No
Time / Place	(四)789 / H371	Language	Chinese

Introduction

This course is intended to introduce and show students how to write hardware de s c r i p t ion in Verilog, and how to write them in a synthesis-friendly style.

Outline

A Tutorial Introduction
Logic Synthesis
Behavioral Modeling
Concurrent Processes
Module Hierarchy
Logic Level Modeling
Cycle-Accurate Specification
Advanced Timing

Prerequisite

Computer Programming Language
Digital Logic